USE NP0 or C0G type decoupling capacitors !!!!!
Solder them on their side !!! to decrease parasitic capacitance

Sheet: FPGA
FPGA_CONFIG_MOSI
FPGA_CONFIG_CCLK
FPGA_CONFIG_INIT_B
FPGA_CONFIG_DONE
FPGA_CONFIG_PROG_B
LOS
ADC_DATA
ADC_BCLK
ADC_LRCLK
TAS3103_BCLK_OUT
TAS3103_DATA_OUT
TAS3103_MCLK_OUT
TAS3103_PLL0
TAS3103_PLL1
TAS3103_MICROCLK_DIV
TAS3103_/RESET
TAS3103_BCLK_IN
TAS3103_LRCLK
TAS3103_DATA_IN
TAS3103_MCLK_IN
ADC_CLIPR
ADC_CLIPL
RESET_ADC
FM_/INT
RESET_FM
FM_DATA
FM_BCLK
FM_LRCLK
PMD100_BCK_OUT
PMD100_LATCH_ENABLE
PMD100_DOL
PMD100_DOR
PMD100_LRCK
PMD100_BCK
PMD100_DATA
PMD100_MCLK
PMD100_HDCD
PMD100_DEEMPH
PMD100_HMUTE
PMD100_FSEL
PMD100_/MEN
PMD100_MDT
PMD100_MS3
PMD100_MS2
PMD100_MS1
DAC_BCK_LEFT+
DAC_LE_LEFT+
DAC_DATA_LEFT+
DAC_BCK_LEFT-
DAC_LE_LEFT-
DAC_DATA_LEFT-
DAC_BCK_RIGHT+
DAC_LE_RIGHT+
DAC_DATA_RIGHT+
DAC_BCK_RIGHT-
DAC_LE_RIGHT-
DAC_DATA_RIGHT-
MCKL_IN
CPU_DAC_BCK
CPU_DAC_LE
CPU_DAC_DATA
CPU_ADC_LE
CPU_ADC_BCK
CPU_ADC_DATA
MCLK
+5V_IN
File: FPGA.sch

Sheet: Filter
SDA
SCL
BCLK_OUT
DATA_OUT
MCLK_OUT
+VIn
+VRef
PLL0
PLL1
MICROCLK_DIV
/RESET
BCLK_IN
LRCLK
DATA_IN
MCLK_IN
File: Filter.sch

Sheet: Digital_Filter
+VIn
+VRef
BCK_OUT
LATCH_ENABLE
DOL
DOR
LRCK_IN
BCK_IN
DATA_IN
MCLK
HDCD
DEEMPH
HMUTE
FSEL
/MEN
MDT
MS3
MS2
MS1
File: Digital_Filter.sch

Sheet: CPU
+VIn
+VRef
MCLK_OUT
DAC_BCLK
DAC_LRCLK
DAC_DATA
SDA
SCL
ADC_LRCLK
ADC_BCLK
ADC_DATA
MCLK_IN
File: CPU.sch

+VIn
TL431CLP
VR1
C
A
R
1k/1%
R1
1k/1%
R2
+VRef
150uF/SANYO OSCON 10SVP150M
C1
5.00R/0.1W
R3

P4
+VIn
VRELAYS
SDA
SCL
RESET
VOL_SETUP_LEFT

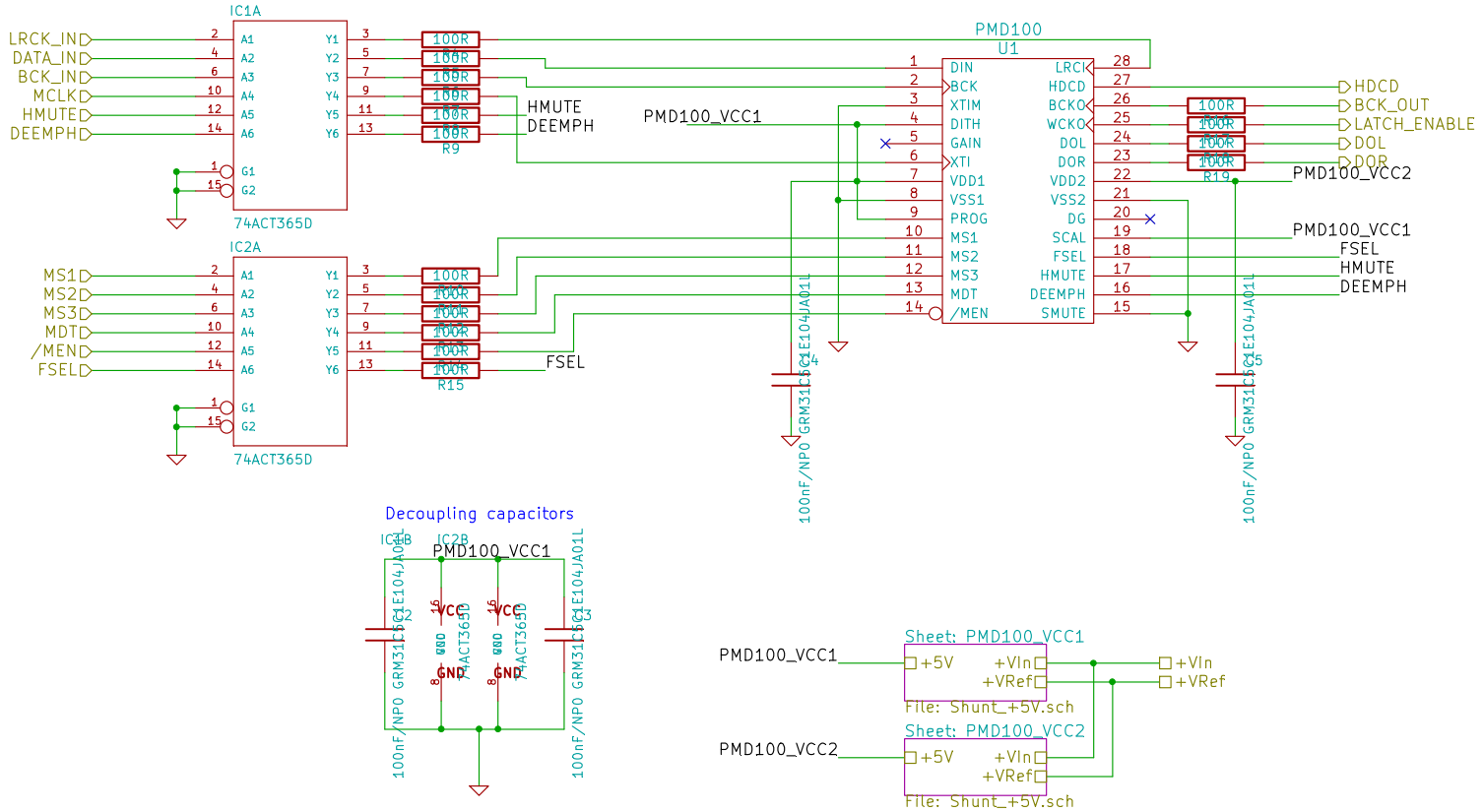
P5
+VIn
VRELAYS
SDA
SCL
RESET
VOL_SETUP_RIGHT

P1
DAC
DAC_BCK_LEFT+
DAC_LE_LEFT+
DAC_DATA_LEFT+
DAC_BCK_LEFT-
DAC_LE_LEFT-
DAC_DATA_LEFT-
DAC_BCK_RIGHT+
DAC_LE_RIGHT+
DAC_DATA_RIGHT+
DAC_BCK_RIGHT-
DAC_LE_RIGHT-
DAC_DATA_RIGHT-
LOS
CPU_RECEIVER_MCLK
CPU_TRANSMITTER_MCLK
FM_MCLK
ADC_MCLK
SDA
SCL
+VIn
50R transmission line

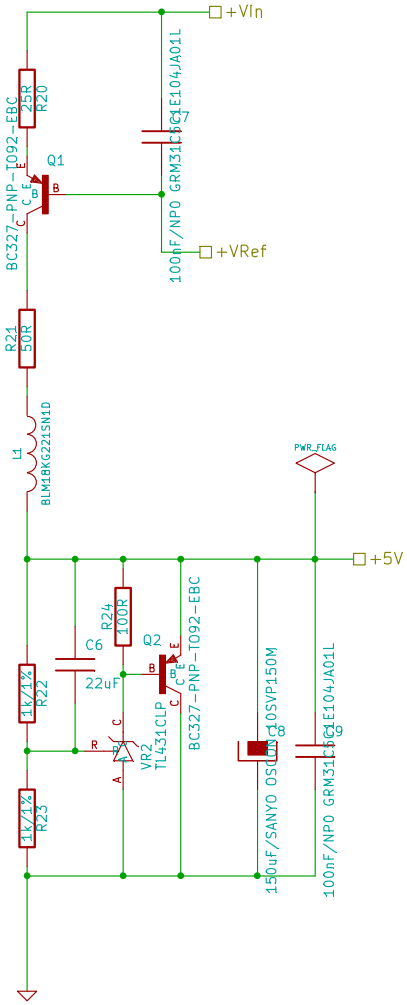
P3
ADC
RESET_ADC
CLIPL
CLIPR
ADC_LE
ADC_BCLK
ADC_DATA
ADC_MCLK

P2
CONN_TUNER
+VIn
AM_SELECT0
AM_SELECT1
FM_RESET
SDA
SCL
FM_INT
FM_DATA
FM_LE
FM_BCK
FM_MCLK

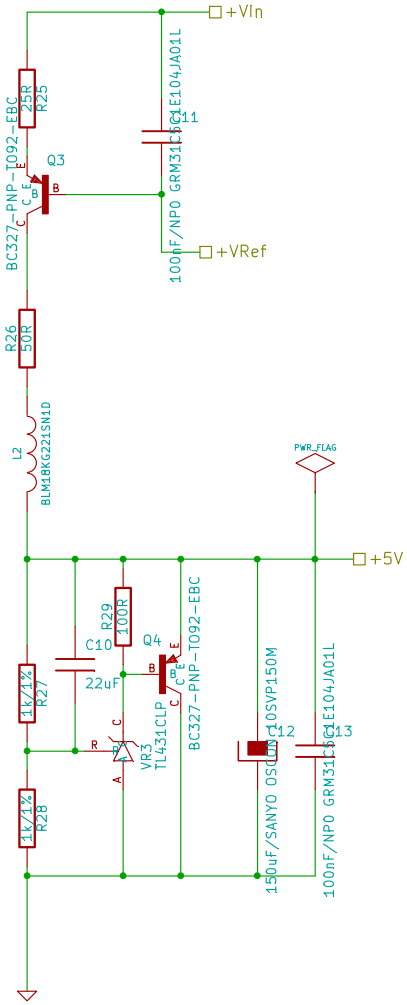
For DIY only. No commercial use allowed
Thierry GRAUSS
File: Motherboard.sch
Sheet: /
Title: Motherboard DAC
Size: A4 | Date: 27 may 2011 | **Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable | Id: 1/18



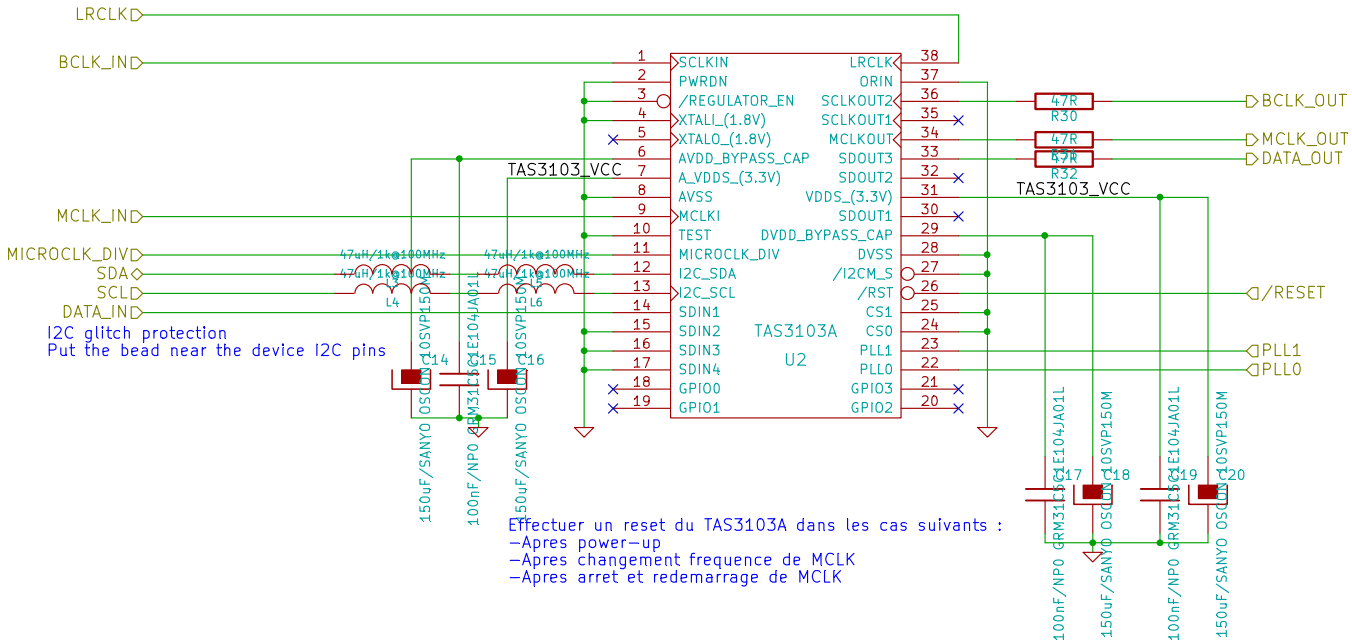
Thierry GRAUSS		
File: Digital_Filter.sch		
Sheet: /Digital Filter/		
Title: PMD100 digital filter		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 2/18



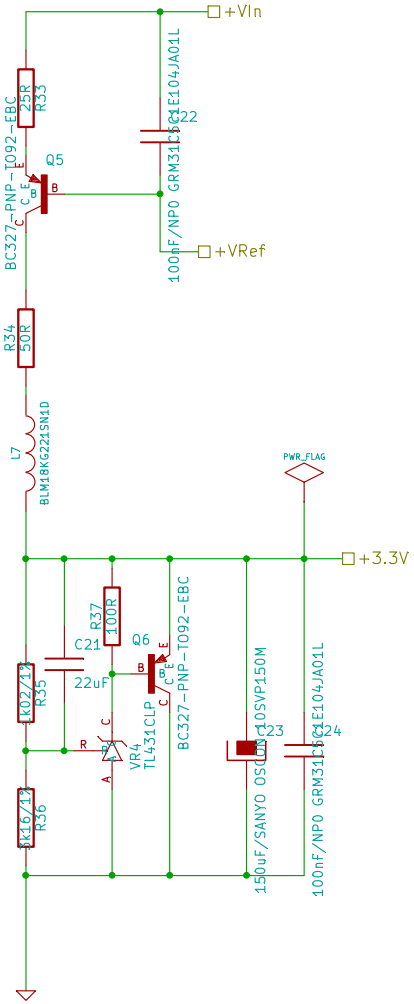
Thierry GRAUSS		
File: Shunt_+5V.sch		
Sheet: /Digital Filter/PMD100_VCC2/		
Title: Shunt regulator +5V		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 3/18



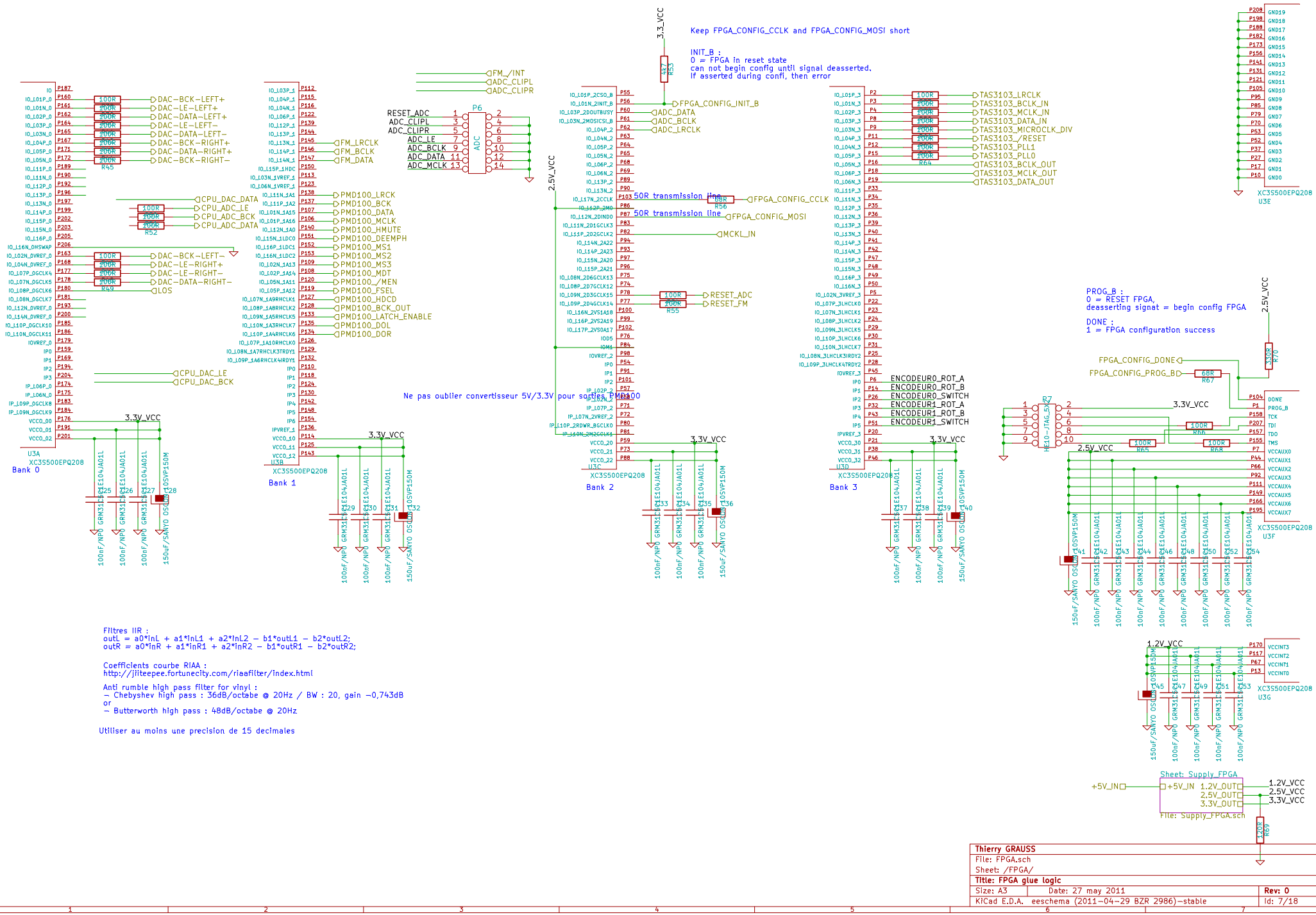
Thierry GRAUSS		
File: Shunt_+5V.sch		
Sheet: /Digital Filter/PMD100_VCC1/		
Title: Shunt regulator +5V		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 4/18



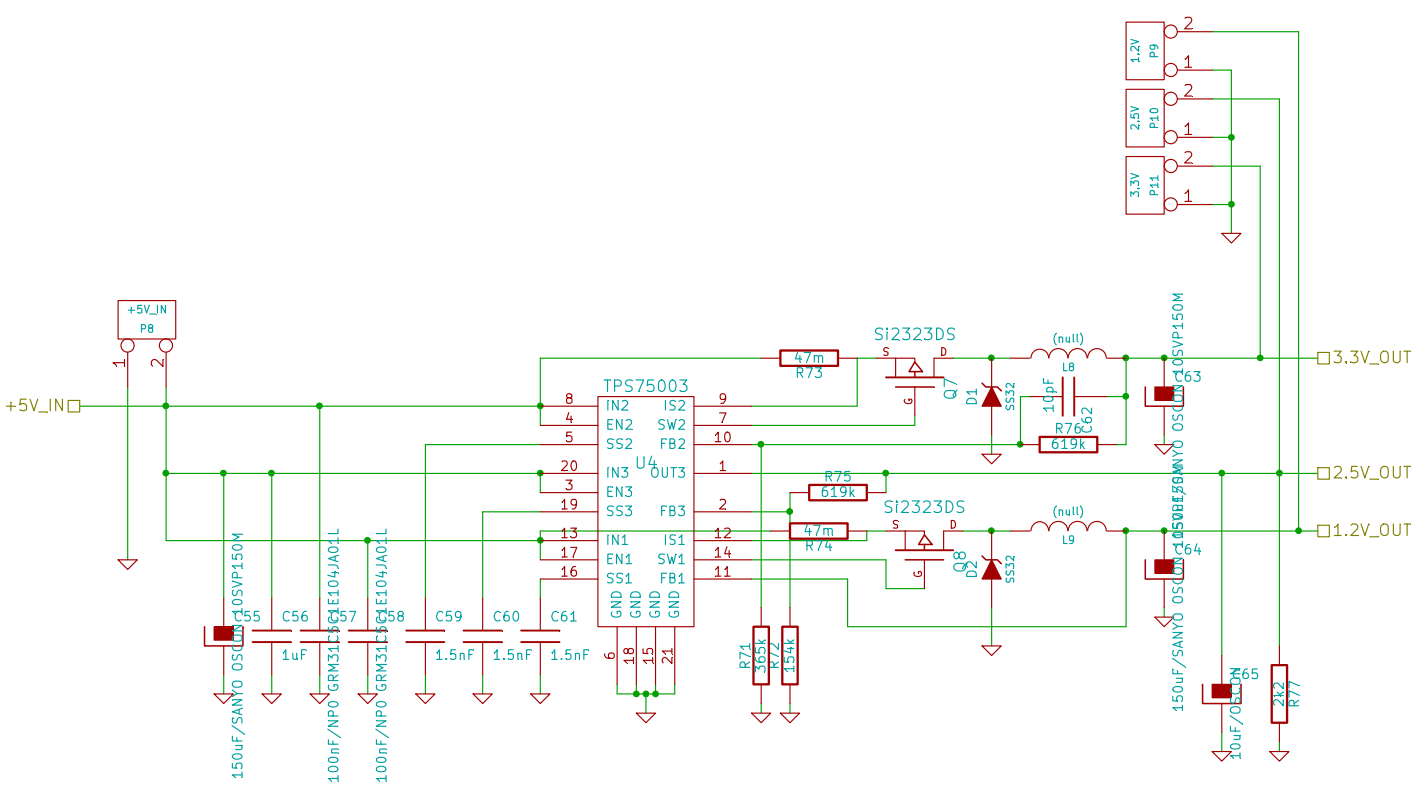
Thierry GRAUSS		
File: Filter.sch		
Sheet: /Filter/		
Title: TAS3103A filter		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 5/18



File: Shunt_+3.3V.sch		
Sheet: /Filter/TAS3103_VCC/		
Title:		
Size: A4	Date: 27 may 2011	**Rev:**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 6/18



Thierry GRAUSS	
File: FPGA.sch	
Sheet: /FPGA/	
Title: FPGA glue logic	
Size: A3	Date: 27 may 2011
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable	Rev: 0
	Id: 7/18



For PCB layout :
http://focus.ti.com/lit/ds/symlink/tps75003.pdf

Thierry GRAUSS		
File: Supply_FPGA.sch		
Sheet: /FPGA/Supply_FPGA/		
Title: FPGA triple power supply		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 8/18

Calcul impedance des pistes : http://www.mantaro.com/resources/impedance_calculator.htm#differential_microstrip_impedance
Regles a respecter pour diminuer EMI : http://www.hottconsultants.com/techtips/red_flags.html
Router USB : http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf
et http://www.atmel.com/dyn/resources/prod_documents/doc7633.pdf

Schematic check list pour AVR32 : http://www.atmel.com/dyn/resources/prod_documents/doc32090.pdf

Place USB host controller, CPU, ethernet and major components on the board
Route high speed diff pairs first and away from clocks and periodic signals and I/O connectors
Minimum length for diff pairs
Minimum number of via and corners for diff pairs
Use 45 degrees angles and not 90 degrees
Do not route diff pairs under/near crystals, oscillators, magnetic devices, IC that use clocks...
Route traces over a solid ground plane
Maintain // for diff pair traces
Diff pairs must have 90R differential impedance
distance of diff pair and periodic signal > 50 mils
distance of diff pairs and non periodic signal traces > 20 mils
length mismatch of diff pairs < 150 mils
put the ESD (PGB0010603MR) diodes as close as possible to the connector

keep traces at least 20*(height over the plane) from the edge of the plane (>90 mils from edge for a 4 layer board)
for a 4 layer board with signal layer on the outside, use 7.5 mils spacing with 7.5 mils traces to give a 90R diff impedance

I2C base address
0x22 : SI4734 /SEN=0
0x30 : left volume
0x31 : right volume
0x68 : TAS3103A
0xAC : SI570

Sheet: ethernet
File: ethernet.sch

Sheet: USB_FTDI
File: USB_FTDI.sch

Sheet: SPI_FERAM
File: SPI_FERAM.sch

Sheet: SRAM
File: SRAM.sch

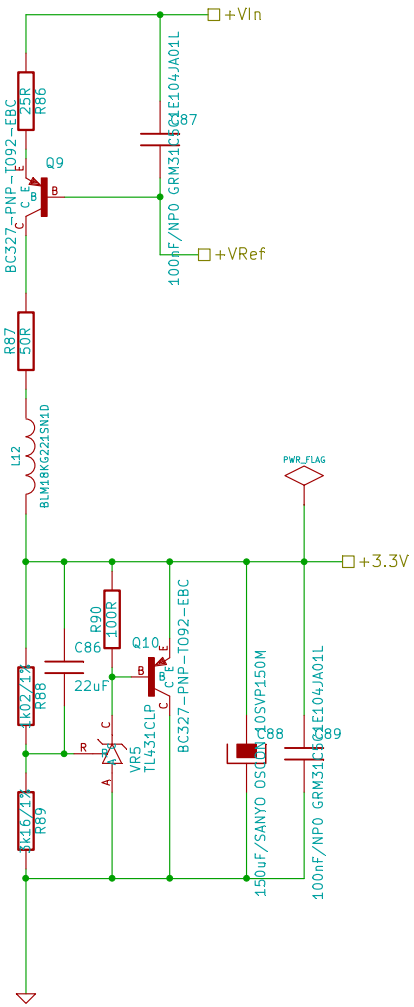
AT32UC3A0512
U5

Close to UC3 pins

Sheet: CPU_VCC
File: Shunt_+3.3V.sch

Decoupling capacitors. For placement,
see : http://www.atmel.com/dyn/resources/prod_documents/doc32090.pdf

Thierry GRAUSS		
File: CPU.sch		
Sheet: /CPU/		
Title: CPU		
Size: A3	Date: 27 may 2011	Rev: 0
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 9/18

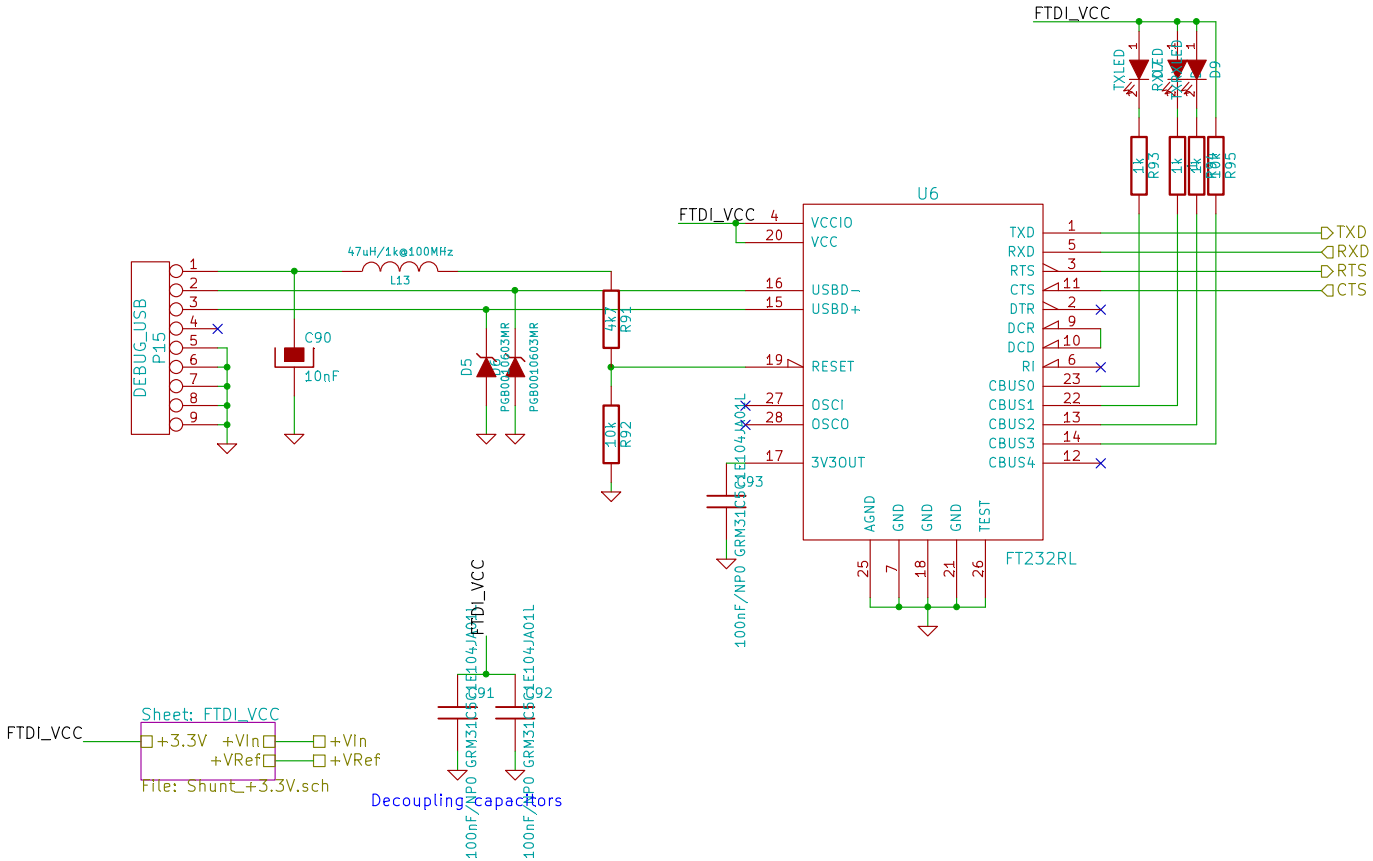


File: Shunt_+3.3V.sch		
Sheet: /CPU/CPU_VCC/		
Title:		
Size: A4	Date: 27 may 2011	**Rev:**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 10/18

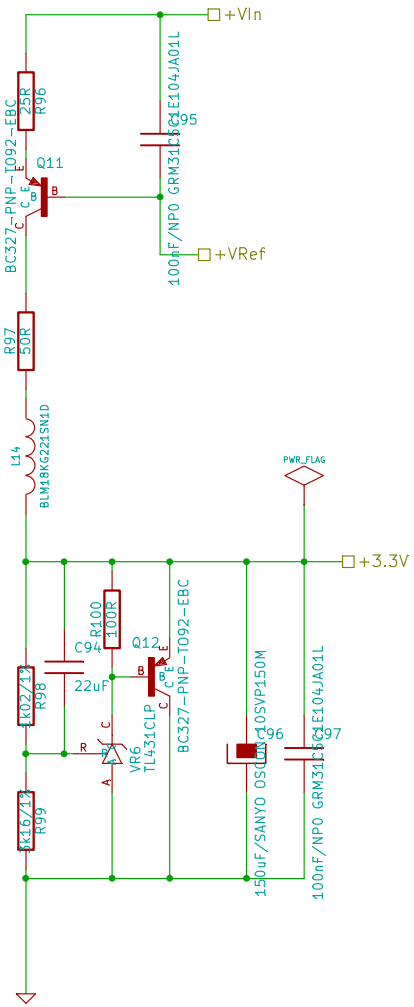
Pour layout PCB USB : cf. http://www.atmel.com/dyn/resources/prod_documents/doc7633.pdf
et http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf

Place USB host controller, CPU, ethernet and major components on the board
Route high speed diff pairs first and away from clocks and periodic signals and I/O connectors
Minimum length for diff pairs
Minimum number of via and corners for diff pairs
Use 45 degrees angles and not 90 degrees
Do not route diff pairs under/near crystals, oscillators, magnetic devices, IC that use clocks...
Route traces over a solid ground plane
Maintain // for diff pair traces
Diff pairs must have 90R differential impedance
distance of diff pair and periodic signal > 50 mils
distance of diff pairs and non periodic signal traces > 20 mils
length mismatch of diff pairs < 150 mils
put the ESD (PGB0010603MR) diodes as close as possible to the connector

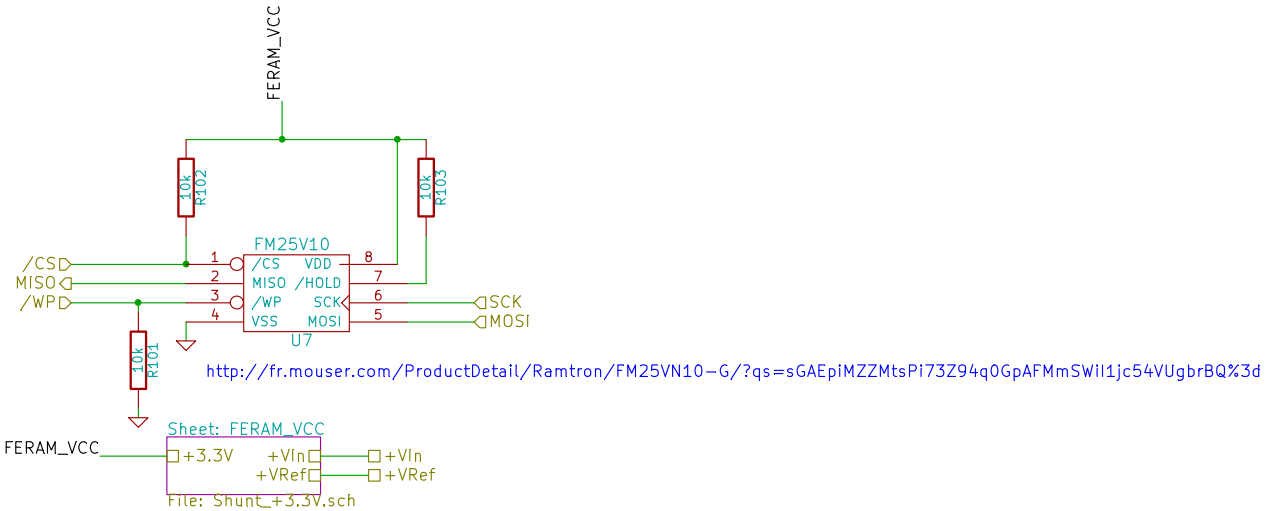
keep traces at least 20*(height over the plane) from the edge of the plane (>90 mils from edge for a 4 layer board)
for a 4 layer board with signal layer on the outside, use 7.5 mils spacing with 7.5 mils traces to give a 90R diff impedance



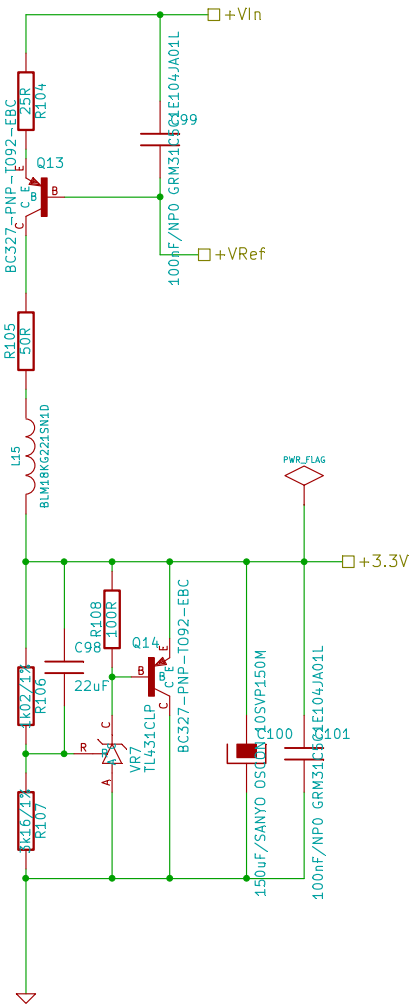
Thierry GRAUSS		
File: USB_FTDI.sch		
Sheet: /CPU/USB_FTDI/		
Title: UDB serial adapter		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 11/18



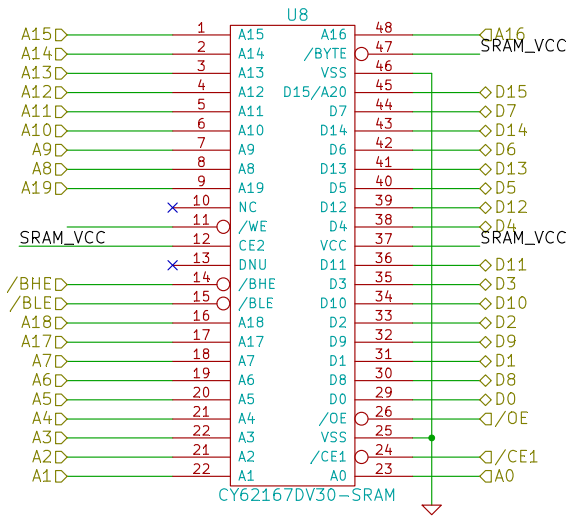
File: Shunt_+3.3V.sch		
Sheet: /CPU/USB_FTDI/FTDI_VCC/		
Title:		
Size: A4	Date: 27 may 2011	**Rev:**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 12/18

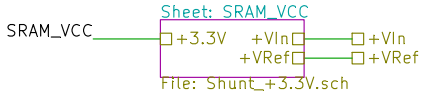


Thierry GRAUSS		
File: SPI_FERAM.sch		
Sheet: /CPU/SPI_FERAM/		
Title: Module FeRAM		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 13/18

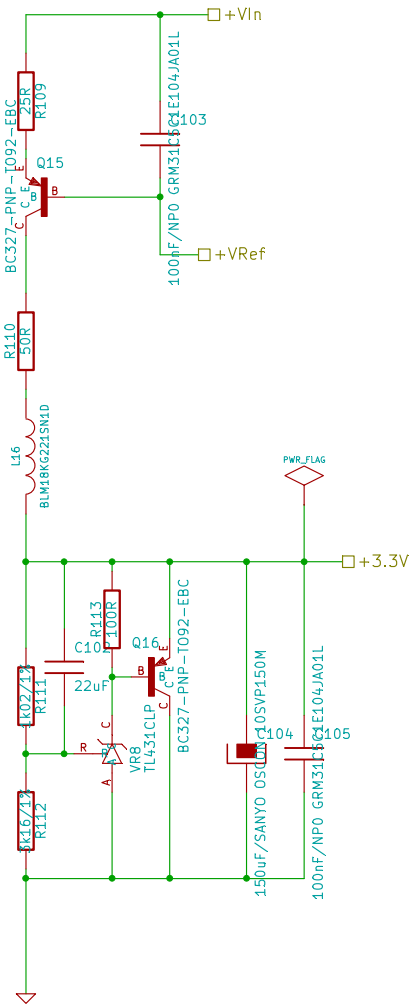


File: Shunt_+3.3V.sch		
Sheet: /CPU/SPI_FERAM/FERAM_VCC/		
Title:		
Size: A4	Date: 27 may 2011	**Rev:**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 14/18

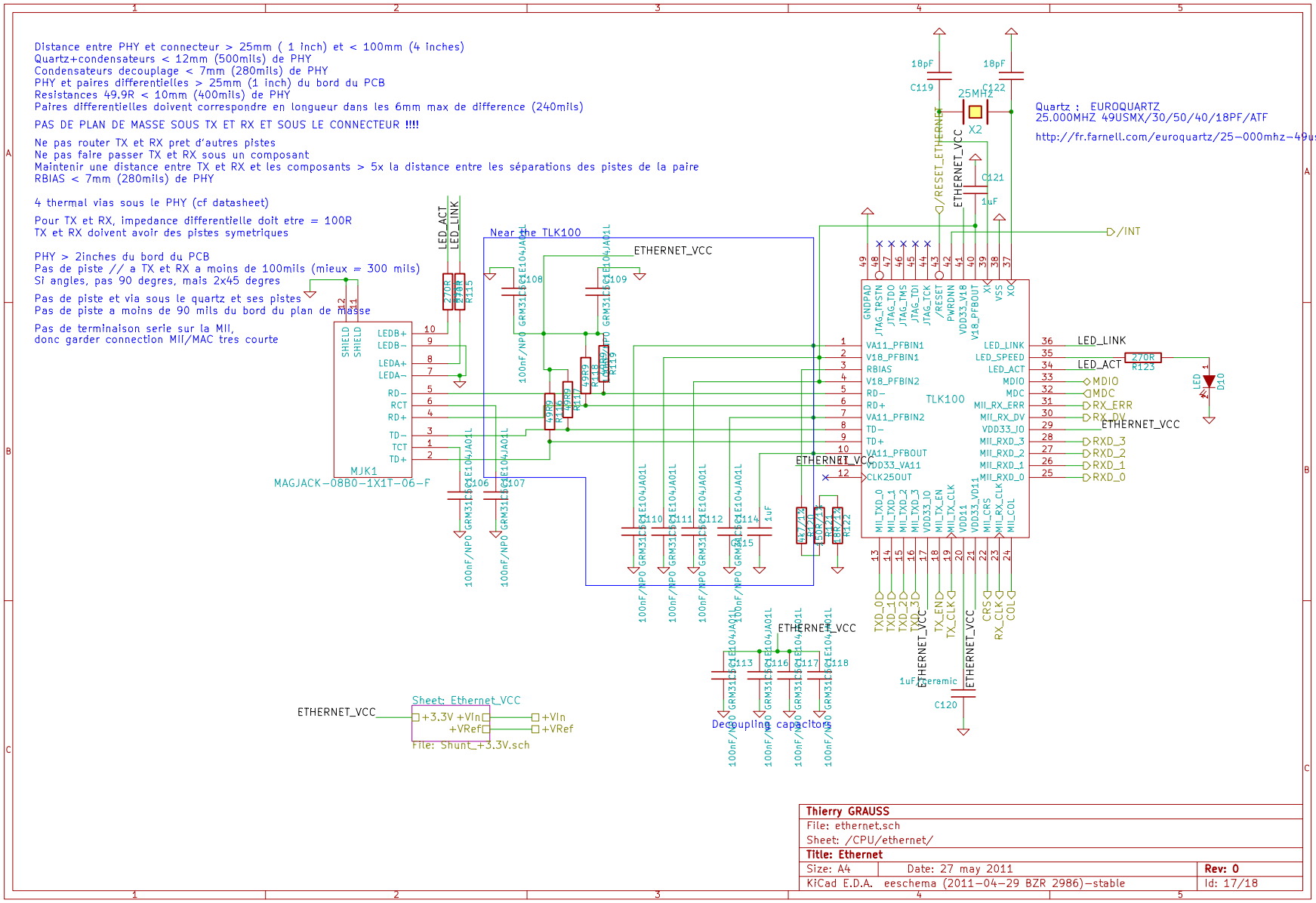


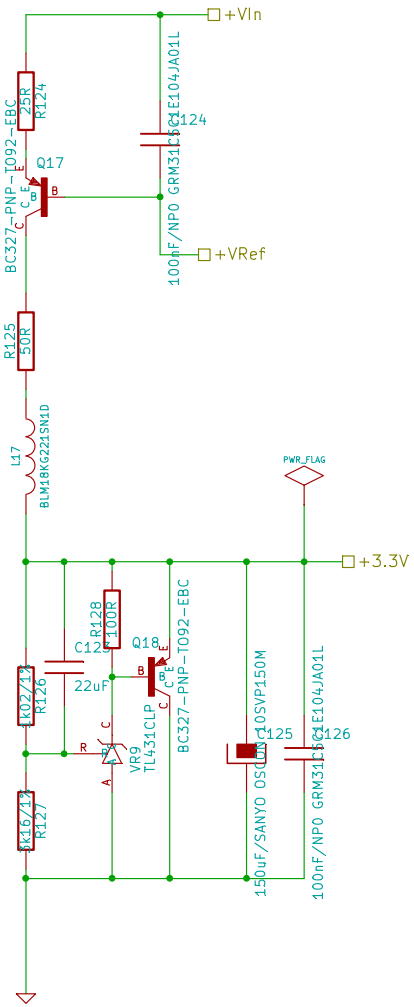


Thierry GRAUSS		
File: SRAM.sch		
Sheet: /CPU/SRAM/		
Title: Module SRAM		
Size: A4	Date: 27 may 2011	**Rev: 0**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 15/18



File: Shunt_+3.3V.sch		
Sheet: /CPU/SRAM/SRAM_VCC/		
Title:		
Size: A4	Date: 27 may 2011	**Rev:**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 16/18


Distance entre PHY et connecteur > 25mm (1 inch) et < 100mm (4 inches)
Quartz+condensateurs < 12mm (500mils) de PHY
Condensateurs decouplage < 7mm (280mils) de PHY
PHY et paires differentielles > 25mm (1 inch) du bord du PCB
Resistances 49.9R < 10mm (400mils) de PHY
Paires differentielles doivent correspondre en longueur dans les 6mm max de difference (240mils)
PAS DE PLAN DE MASSE SOUS TX ET RX ET SOUS LE CONNECTEUR !!!!
Ne pas router TX et RX pret d'autres pistes
Ne pas faire passer TX et RX sous un composant
Maintenir une distance entre TX et RX et les composants > 5x la distance entre les séparations des pistes de la paire
RBIAS < 7mm (280mils) de PHY
4 thermal vias sous le PHY (cf datasheet)
Pour TX et RX, impedance differentielle doit etre = 100R
TX et RX doivent avoir des pistes symetriques
PHY > 2inches du bord du PCB
Pas de piste // a TX et RX a moins de 100mils (mieux = 300 mils)
Si angles, pas 90 degres, mais 2x45 degres
Pas de piste et via sous le quartz et ses pistes
Pas de piste a moins de 90 mils du bord du plan de masse
Pas de terminaison serie sur la MII,
donc garder connection MII/MAC tres courte
Quartz : EUROQUARTZ
25.000MHZ 49USMX/30/50/40/18PF/ATF
http://fr.farnell.com/euroquartz/25-000mhz-49usmx-30-50-40-18pf-atf/crystal-25-000mhz/dp/1640907
18pF
C119
18pF
C122
25MHz
X2
/RESET_ETHERNET
ETHERNET_VCC
C121
1uF
/INT
LED_ACT
LED_LINK
Near the TLK100
ETHERNET_VCC
270R
R123
LED
D10
MJK1
MAGJACK-08B0-1X1T-06-F
TLK100
MDIO
MDC
RX_ER
RX_DV
RXD_3
RXD_2
RXD_1
RXD_0
TXD_0
TXD_1
TXD_2
TXD_3
TX_EN
TX_CLK
CRS
RX_CLK
COL
1uF Ceramic
C120
Sheet: Ethernet_VCC
+3.3V +VIn
+VRef
File: Shunt_+3.3V.sch
Decoupling capacitors
Thierry GRAUSS
File: ethernet.sch
Sheet: /CPU/ethernet/
Title: Ethernet
Size: A4
Date: 27 may 2011
Rev: 0
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable
Id: 17/18



File: Shunt_+3.3V.sch		
Sheet: /CPU/ethernet/Ethernet_VCC/		
Title:		
Size: A4	Date: 27 may 2011	**Rev:**
KiCad E.D.A. eeschema (2011-04-29 BZR 2986)-stable		Id: 18/18